High Voltage Step-Down White LED Driver

REV: 00a

General Description

The LD7850 is a step-down DC/DC converter, especially designed to drive power white LEDs with constant current. With capability to transfer output voltage up to 60V, the LD7850 can drive a string of up to 15 series-connected power white LEDs and ensure uniform brightness. To optimize the efficiency, the feedback voltage is set to 0.4V. This reduces the power dispassion on the current sense resistor. The other features include under-voltage lockout, over-current protection and dimming function essential for the white LED applications.

LD7850 is available in a space saving MSOP-10 and SOP-8 package.

+patent pending

Features

- Input Voltage Range: 12V to 70V
- Hysteresis Mode Control
- Drive one string of LEDs, V_O up to 60V
- No need output capacitor
- Analog Dimming Control
- Over Current Protection
- Suspend current < 1.5mA

Applications

- Electronic Appliances
- Automotive LED Driver Application
- Bracket Lamp and Wall Lamp Application

Typical Application

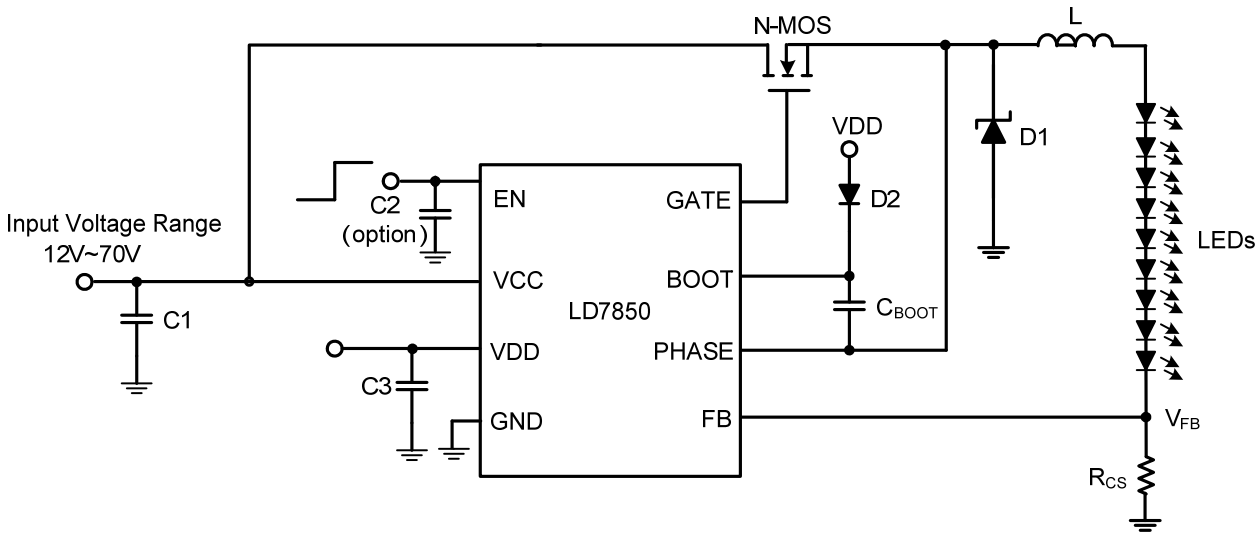
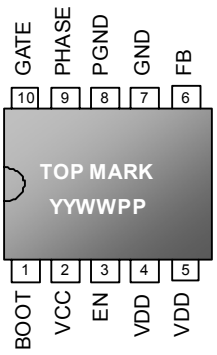


Fig. 1 Application circuit

Pin Configuration

SOP-8 (EP) (TOP VIEW)

MSOP-10 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		TOP MARK	Shipping
LD7850 GSE	SOP-8 (EP)	Green Package	LD7850GSE	2500 /tape & reel
LD7850 GL	MSOP-10	Green Package	7850GL	2500 /tape & reel

Note: The LD7850 is ROHS compliant.

Pin Descriptions

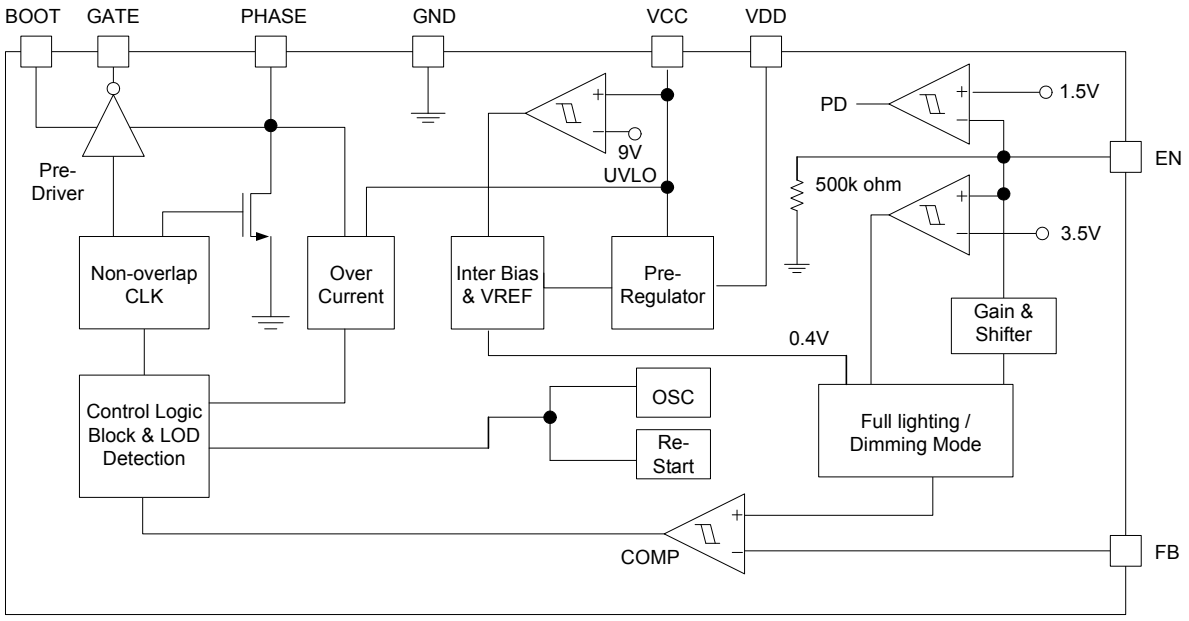
SOP-8 (EP)

PIN	NAME	FUNCTION
1	BOOT	This pin provides ground referenced bias voltage to the high-side MOSFET driver. Connect this pin to a bootstrap circuit to pump boot voltage to drive an N-MOS.
2	VCC	Supply Voltage Input. VCC supplies power to Step-down converter. Bypass this pin to GND with a ceramic capacitor of at least 10μF.
3	EN	This pin provides both Enable and Dimming functions. Enable Function. High=enable, Low=Disable. Dimming can be accomplished by applying analog signal to EN pin. If EN pin floats, a fault protection detector will disable the chip.
4	VDD	Internal Regulator Output Voltage. Bypass this pin to GND with a 1μF ceramic capacitor. This pin provides the bias for the control circuitry and the high-side N-MOS driver.
5	FB	Feedback Pin. Connect a resistor from FB to ground to set the LED current.
6	GND	IC GND.
7	PHASE	Inductor switching node. Connect to Inductor and bootstrap flying capacitor.
8	GATE	Gate drive output to drive the high-side N-MOS.

MSOP-10

PIN	NAME	FUNCTION
1	BOOT	This pin provides ground referenced bias voltage to the high-side MOSFET driver. Connect this pin to a bootstrap circuit to pump a boot voltage to drive an N-MOS.
2	VCC	Supply Voltage Input. VCC supplies power to Step-down converter. Bypass this pin to GND with a ceramic capacitor of at least 10μF.
3	EN	This pin provides both Enable and Dimming functions. Enable Function. High=enable, Low=Disable. Dimming can be accomplished by applying either analog or PWM signal to EN pin, subject to different applications. If EN is floating, a fault protection detector will disable the chip.
4, 5	VDD	Internal Regulator Output Voltage. Bypass this pin to GND with a 1μF ceramic capacitor. This pin provides the bias for the control circuitry and the high-side N-MOS driver.
6	FB	Feedback Pin. Connect a resistor from FB to ground to set the LED current.
7, 8	GND	IC GND.
9	PHASE	Inductor switching node. Connect to Inductor and bootstrap flying capacitor.
10	GATE	Gate drive output to drive the high-side N-MOS.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V~75V
BOOT Pin to GND	-0.3V~82V
PHASE Pin to GND	-1.0V~75V
BOOT Pin to PHASE Pin	-0.3V~7.5V
VDD Pin	-0.3V~7.5V
FB and EN to GND	-0.3V~7V
GATE	V_{PHASE}-0.3V~V_{BOOT}+0.3V
Gate Output Current	500mA
Operating Temperature Range	-40°C to 100°C
Storage Temperature Range	-55°C to 125°C
Package Thermal Resistance SOP-8 (EP) θ_{JA}	50°C/W
Package Thermal Resistance MSOP-10 θ_{JA}	160°C/W
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec)	260 °C
ESD Level (Human Body Model)	2kV
ESD Level (Machine Model)	200V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=30V, EN=5V, 4LED, I_{LED}=350mA)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage VCC		12		70	V
UVLO (ON)		8.5	9.5	10.5	V
UVLO (OFF)		8.0	9.0	10	V
Suspend Current	EN=0, VCC=30V		820	1500	μA
Quiescent Current, I_Q	FB=1.0V, EN>4V		1.5	2.0	mA
VDD Internal Voltage Regulator		6.7	7.1	7.5	V
FB					
Reference Voltage			400		mV
Reference Voltage Tolerance	(Note 1)	-3.0		3.0	%
Hysteresis Window			±56		mV
Gate/Phase					
Driver Capacity	VDD=7.1V, Output High (P-side)		10	20	Ω
	VDD=7.1V, Output Low (N-side)		10	20	Ω
Low Side Driver Resistance			50		Ω
EN					
EN Voltage Threshold	Enable	1.3			V
	Disable			0.7	V
	Full Lighting Mode	3.5	4.0		V
Impedance to GND					
EN Pin to GND			500		kΩ
Over current trip point					
VCC-V_{PHASE}	VCC=10V	0.8	1.0	1.2	V

Note 1: It is case sensitivity, especially in higher voltage input combined with lower output LED current case.

Typical Performance Characteristics

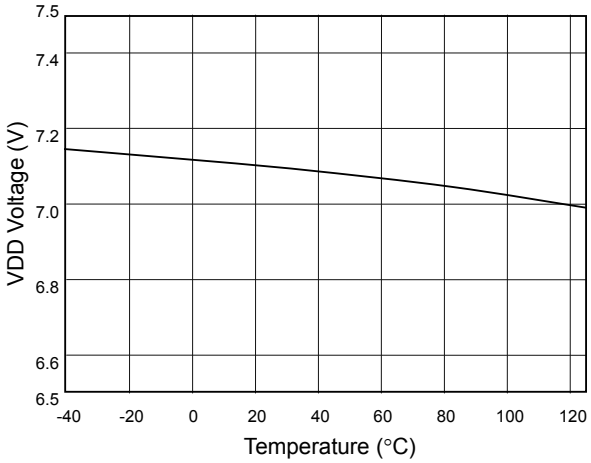


Fig. 2 VDD Voltage vs. Temperature

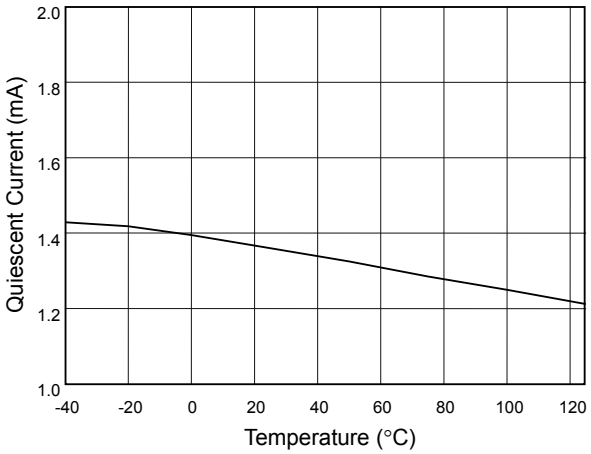


Fig. 3 Quiescent Current vs. Temperature

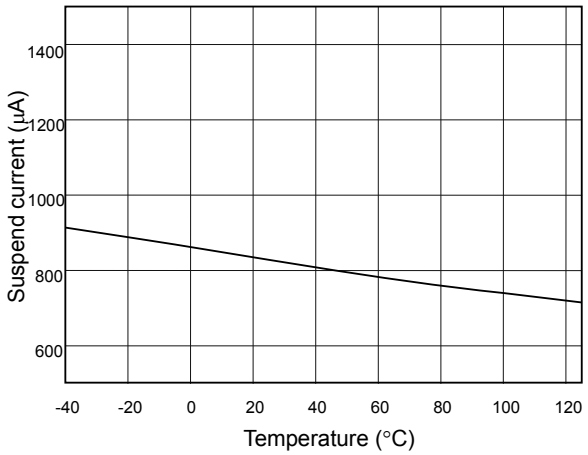


Fig. 4 Suspend current vs. Temperature

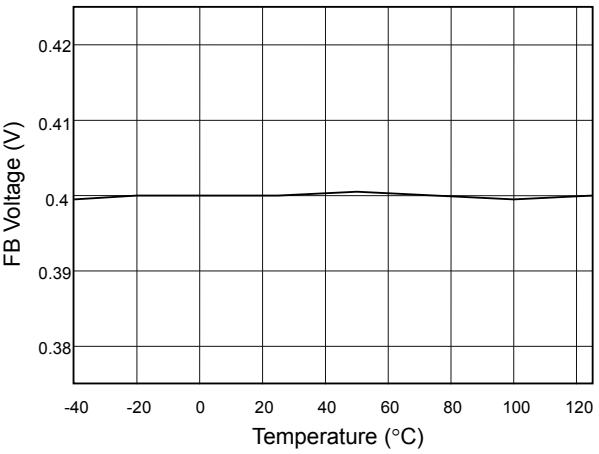


Fig. 5 FB Voltage vs. Temperature

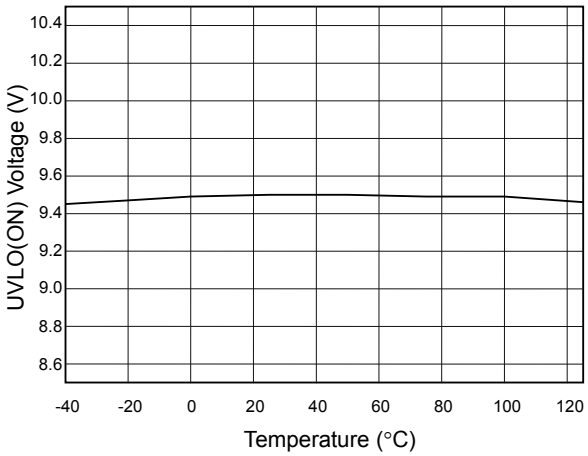


Fig. 6 UVLO(ON) Voltage vs. Temperature

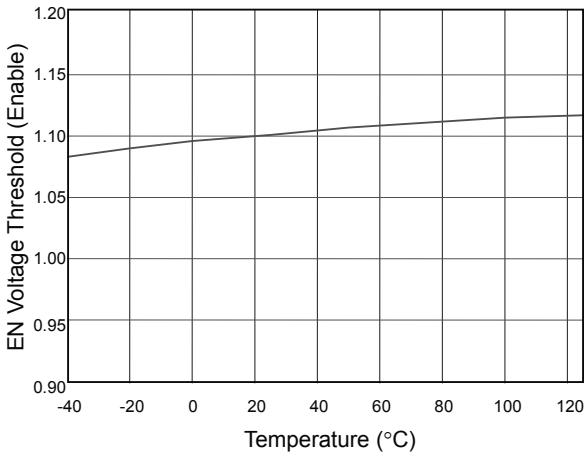


Fig. 7 EN Voltage Threshold vs. Temperature

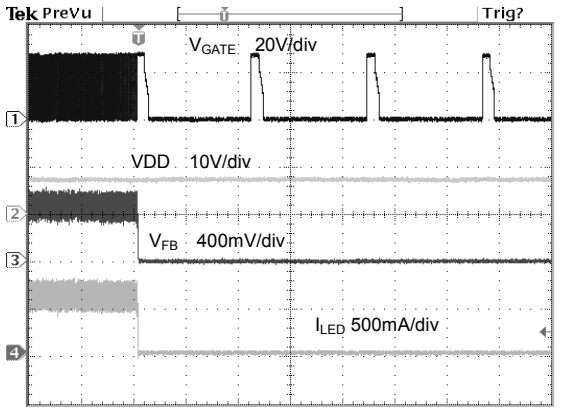


Fig. 8 LED Open Circuit Waveform

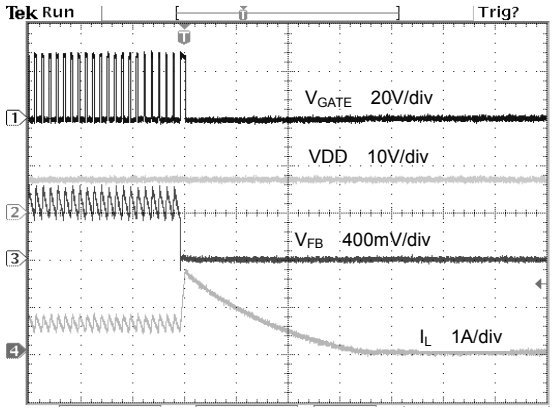


Fig. 9 Over Current Protection Function

Application Information

LED Current Program

The LED current is programmed by the feedback resistor (R_{CS} in Fig.1). Where the feedback reference is 0.4V, the current for driving LEDs could be determined by the following formula:

$$I_{LED} = \frac{0.4V}{R_{CS}}.$$

In order to obtain accurate LED current, it is preferred to use a feedback resistor with higher precision (of 1% is strongly recommended).

Analog Dimming Control

The analog dimming can be achieved by applying to the EN pin a voltage of a voltage level from 1.5V~3.5V to adjust the averaged LED current. Pulling EN pin high above 4.0V will achieve the maximum brightness.

Over Current Protection (OCP)

The voltage difference between VCC and Phase pins will trigger OCP if it is higher than 1.0V. Thus, IOCP, the threshold current for triggering OCP, can be set as follows:

$$I_{OCP} = \frac{1.0V}{R_{DS(ON)}}$$

Where, RDS denotes the turn-on resistance of the power N-MOS. The threshold current is unchangeable no matter it is under a fault condition other than an over-current condition. Once the over-current condition is detected, the IC will be latched off and stop switching to protect the power N-MOS and white LEDs.

If it's required to lower the maximum allowable current peak through the N-MOS at over-current condition, a resistor RADD, as shown in Fig. 10, can be added between VCC pin and the drain of the N-MOS.

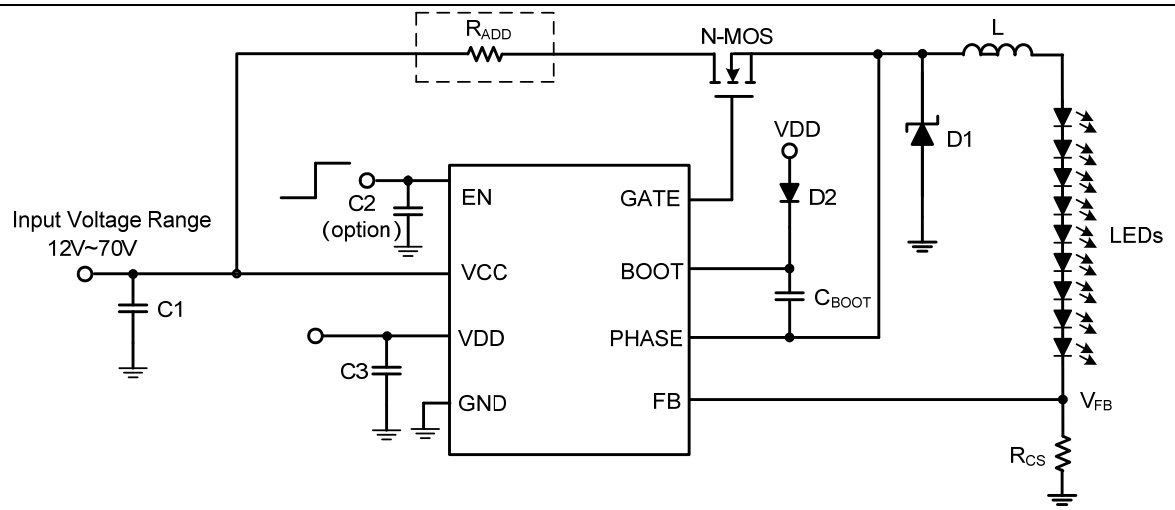


Fig.10

From the above application, the equation for I_{OCP} can be revised as below.

$$I_{OCP} = \frac{1.0V}{R_{DS(ON)} + R_{ADD}}$$

Select an N-MOS that is capable to handle I_{OCP} without inducing current breakdown when approaching the highest operation temperature.

The external N-MOS of large C_{oss} (typical>60pF) can efficiently reduce noise between VCC pin and PHASE pin and prevent the OCP from false triggering.
If necessary, users can put a capacitor between the drain and source of N-MOS to enhance the anti-noise capability.

Shutdown Mode

The LD7850 will enter shutdown mode when the EN voltage is logic low for more than 11ms. During shutdown, the suspend current for the device is less than 1.5mA (max).

Bootstrap Capacitor Selection

In order to drive the external high-side N-MOS effectively, users are required to connect a bootstrap capacitor from BOOT pin to PHASE pin. In further, capacitance at least greater than 10 times C_{ISS} of high-side N-MOS is recommended to achieve optimum design.

Inductor Selection

The inductor is selected to enhance the overall efficiency. Higher value of inductance will reduce the current ripple and minimize the inaccuracy of output current, caused by propagation delay from higher input voltage, lower output voltage, or light load situation. So, the inductance value for LD7850 is recommended in the range from 100μH to 780μH. Furthermore, lower series resistance of inductor will improve the overall efficiency.

The current rating of the inductor is also a concern in design. It's recommended to select inductors with proper rating at least equal to or higher than OCP level.
Select an inductor that is capable to handle over-current without going into saturation when approaching the highest operation temperature.

Operating frequency

For a given duty cycle D, both of inductance and switching frequency would determine the inductor ripple current, which is

$$\frac{1}{f} = \frac{T_D}{D(1-D)} \times (\frac{\Delta V}{\Delta V_{TD}})$$

$$\Delta I_L = \frac{V_O}{f \times L} \times (1 - \frac{V_O}{VCC})$$

Where f is the switching frequency

$$\Delta V_{TD} = \frac{VCC}{L} \times T_D \times R_{CS}$$

$$\Delta V = \Delta V_{TD} + \Delta V_{HYST}$$

T_D is the delay time of the signal path

ΔV_{TD} is the voltage ripple due to the delay time.

ΔV_{HYST} is the hysteresis of comparator.

ΔV is the total voltage ripple due to delay time and hysteresis of comparator.

The peak inductor current is:

$$\Delta I_{LPEAK} = I_O + \frac{\Delta I_L}{2}$$

Where ΔI_L is the inductor peak-to-peak current ripple

The hysteresis window is between ±56mV. Delay time of the signal path is equal to 245ns

Example:

VCC=50V, V_O=32V (to drive 8 WLEDs), L=220μH, I_{LED}=350mA,

$$\Delta V = \Delta V_{TD} + \Delta V_{HYST} = 63.63mV + 112mV = 175.63\,mV$$

$$f = \frac{D(1-D)}{T_D} \times \frac{\Delta V_{TD}}{\Delta V} = 340.706\,kHz$$

$$\Delta I_L = 153.692\,mA$$

∗The recommended operating frequency is between 20kHz and 450kHz for LD7850.

Input Voltage

Regardless of the voltage drop of the N-MOS during N-MOS turn-on, the duty-cycle calculation equation can be written as below,

$$D = \frac{V_O + V_{FD}}{VCC}$$

Where:

$$V_O = N \cdot V_{LED} + V_F$$

N is the number of LEDs.

V_{LED} is the forward conduction voltage of LED (V), and V_{FD} is the forward conduction voltage of schottky diode (V).

Input capacitor Selection

The input capacitor must be connected to the VCC pin of LD7850 to maintain steady input voltage and filter out the pulsing input current. A capacitor of low ESR is required here to minimize the noise. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. It may be necessary in some designs to add a small valued ceramic type capacitor in parallel with the input capacitor to prevent from ringing.

Since the input current is discontinuous in a buck converter, the current stress over the input capacitor is the concern when selecting the capacitor. For a buck converter, the RMS value of the input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \sqrt{\frac{V_O}{VCC} \cdot \left(1 - \frac{V_O}{VCC}\right)}$$

It indicates that when V_O=1/2 VCC, CIN is under the worst case of current stress, that is $0.5I_O$.

Output Capacitor

The LD7850 features hysteresis control method for LED current. An additional output capacitor here would produce inrush current during start-up. **Therefore it's not recommended to connect an output capacitor to the buck converter output terminal**, and so to eliminate the delay effect. The control of the LED current would then perform more precisely and it would save the board space and components.

Layout Consideration

- Keep the VDD bypass capacitor of 1μF very close to IC. (<5mm)
- Keep the EN bypass capacitor of 0.1μF (option) very close to IC.
- Keep the VCC bypass capacitor of at least 10μF very close to IC. (<5mm)

- Keep the buck converter diode and inductor close to the PHASE pin and no via is necessary.
- Locate the feedback resistor as close to their associated pins as possible. And route away from switching nodes, such as PHASE, BOOT and GATE pins.
- Keep the high current path wide and short as possible.

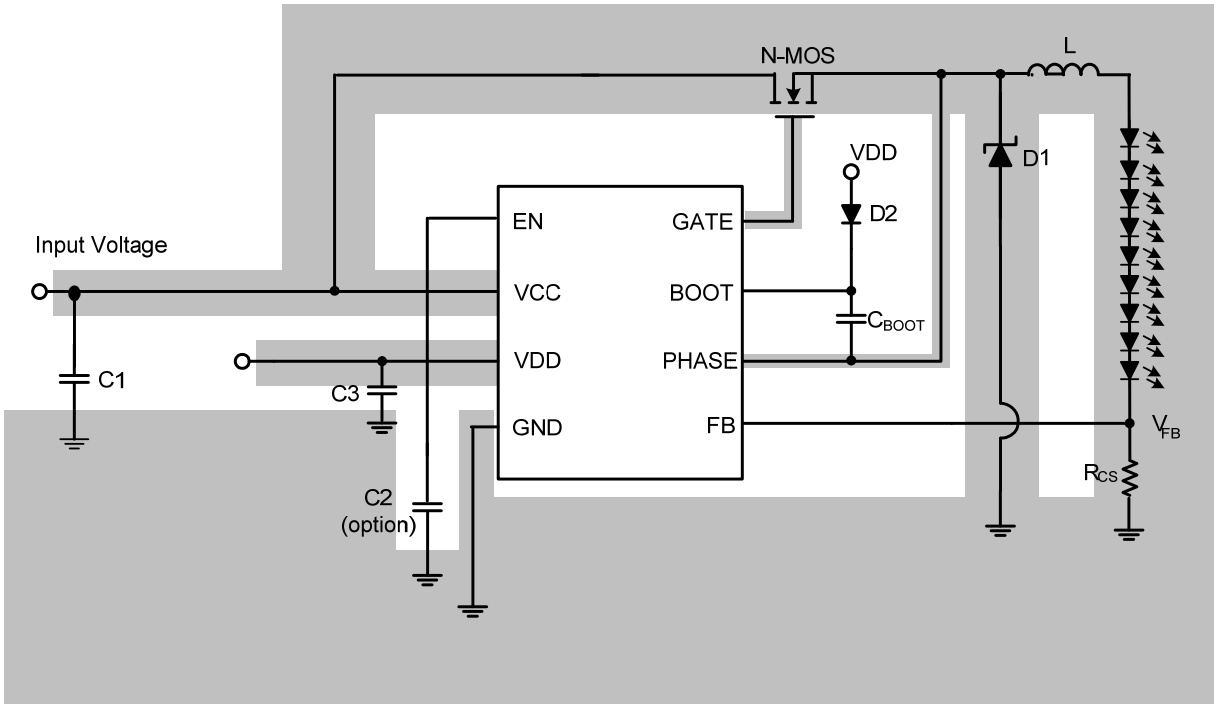


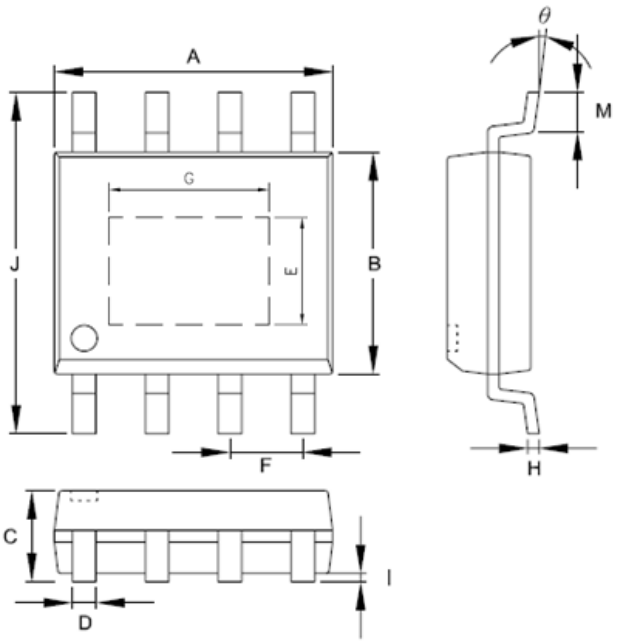
Fig.11 Recommended PCB Layout

BOM list (V_{CCMAX}=70V, I_{LED}=330mA, 6-WLEDs)

REF	Value	PART NO.	Package	Vendor
		LD7850	MSOP-10	Leadtrend
C1	22μF/100V			Rubycon
C2(Option)	0.1μF/X5R/16V		0603	
C3	1μF/X5R/16V		0603	
C_{BOOT}	47nF/X7R/25V		0603	
D1	100V/1A	SBM110PT	SMB	CHENMKO
D2	80V/250mA	MMBD4448BPT	SOD-123	CHENMKO
L	220μH/0.8A	GDO0804-221M	0804	GOTREND
R_{CS}	1.2Ω		0805	
N-MOS	100V/3.2A	AP9997GK	SOT-223	APEC

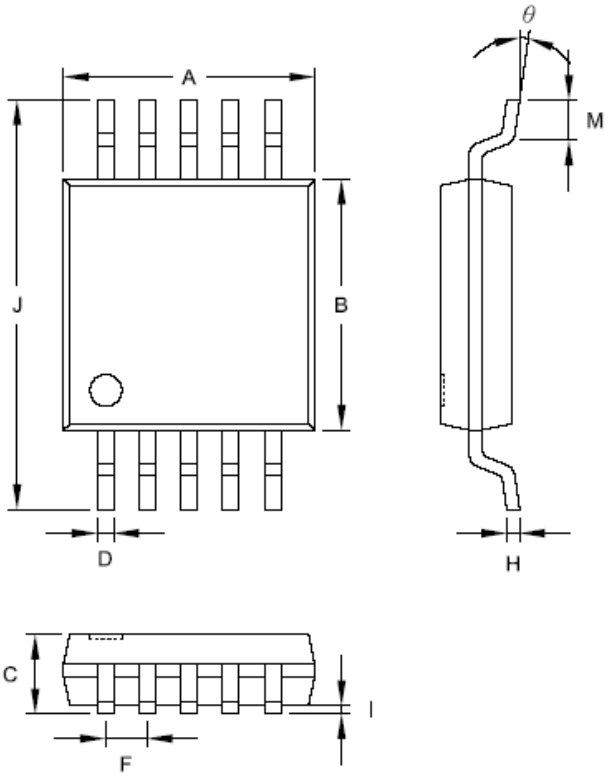
Package Information

SOP-8 (EP)



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
E	1.9	2.7	0.075	0.106
F	1.194	1.346	0.047	0.053
G	1.9	3.6	0.075	0.142
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

MSOP-10

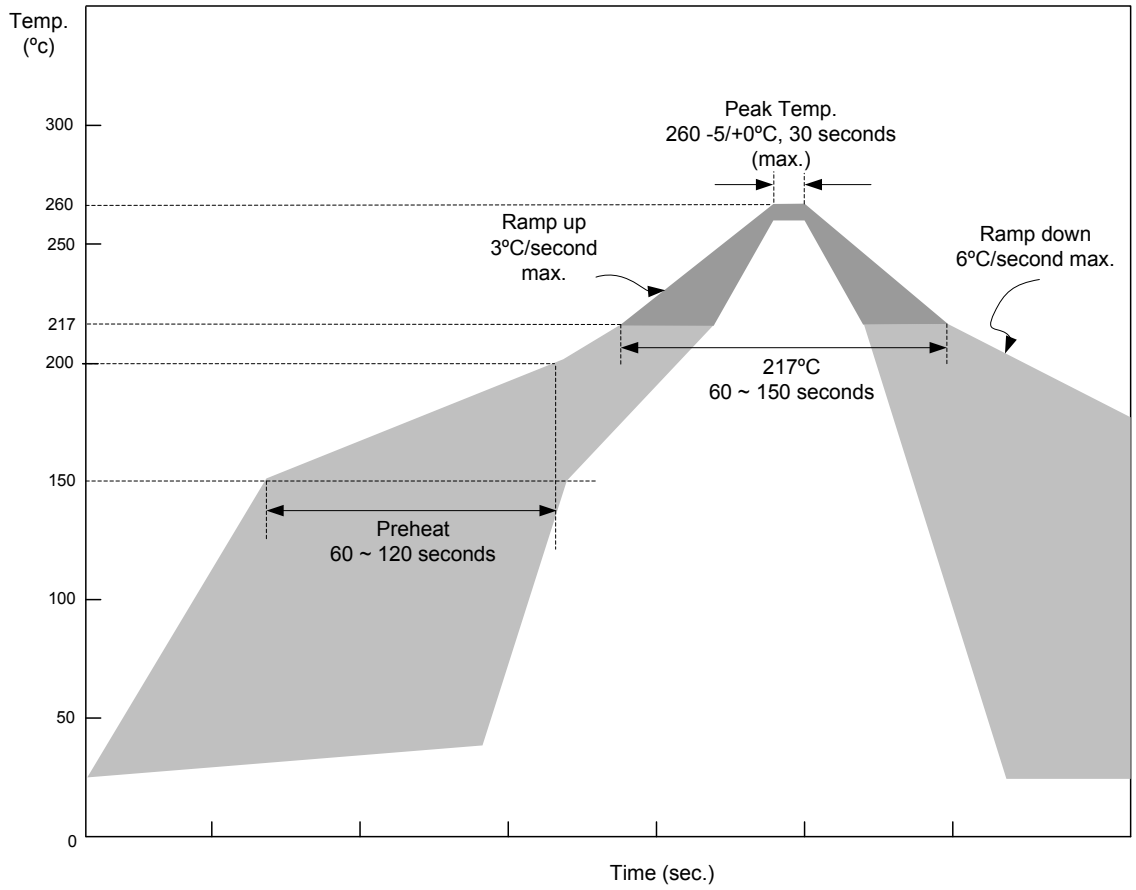


Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	2.896	3.099	0.114	0.122
B	2.896	3.099	0.114	0.122
C	0.813	1.219	0.032	0.048
D	0.152	0.305	0.006	0.012
F	0.470	0.530	0.019	0.021
H	0.127	0.229	0.005	0.009
I	0.051	0.152	0.002	0.006
J	4.699	5.105	0.185	0.201
M	0.406	0.660	0.016	0.026
θ	0°	6°	0°	6°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

IR Profile for SMD Devices



Item	Average Ramp-up Rate	Pre-heat (150 ~ 200°C)	Time Maintained Above 217°C	Peak Temp.	Ramp-down Rate
Required	3°C(max) /sec	60~120 sec	60~150 seconds	260 +0/-5°C 30 seconds	6°C (max) /sec

Revision History

Rev.	Date	Change Notice
00	4/21/2009	Original Specification
00a	3/18/2010	Package option: SOP-8 (EP)